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In the Abstract:

Please replace the current Abstract with the Abstract attached on a separate page, page no. 2A.

ABSTRACT

A data management architecture for a high speed packet switch has a dual key-based content addressable memory (CAM)-based buffer access control mechanism that stores relatively long data packets for delivery to multiple output ports of the switch. The CAM stores multiple address pointer words, each having a key field to identify a data packet, and an address field to identify the address of the location of the packet buffer in which the data packet is stored. During a CAM search, a packet request key is coupled to the key fields of all address pointer words stored in the CAM. The location of the matching key is used to access the key field's companion address field in its address pointer word to access a data packet stored in the packet buffer, and to address fields of all address pointer words stored in the CAM. The CAM outputs a signal that indicates whether or not the buffer address from which the packet has been accessed is free to store new data.